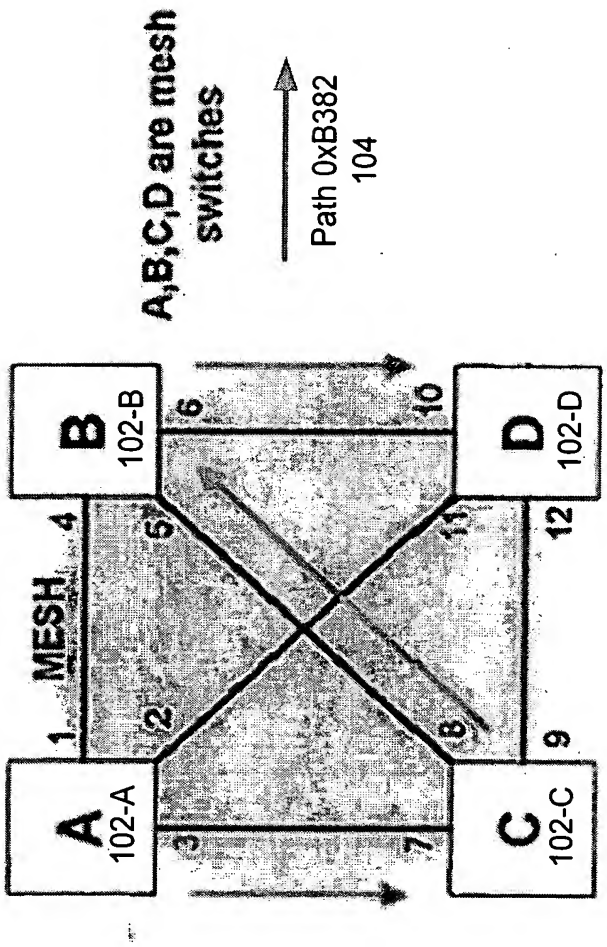

A,B,C,D are mesh switches
Path 0xB382
104
MESH
A
102-A
B
102-B
C
102-C
D
102-D
1
2
3
4
5
6
7
8
9
10
11
12

FIG. 1

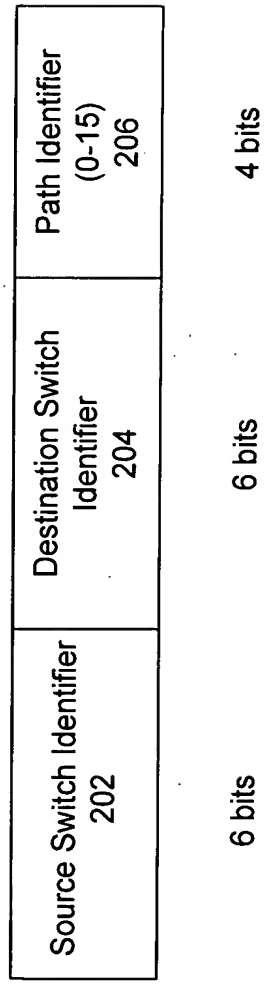

Source Switch Identifier
202
Destination Switch
Identifier
204
Path Identifier
(0-15)
206
6 bits
6 bits
4 bits

FIG. 2

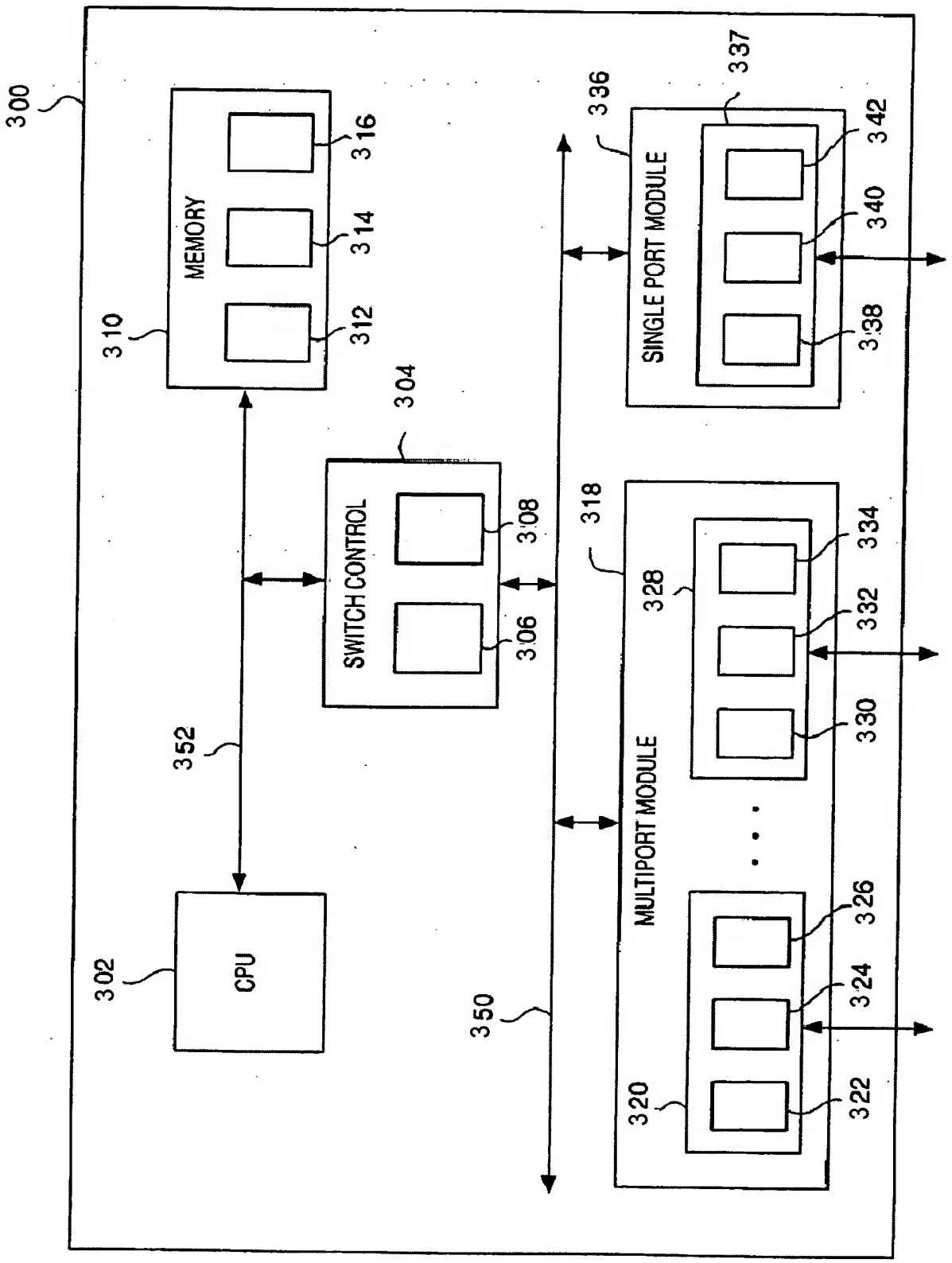

300
MEMORY
316
314
312
310
304
SWITCH CONTROL
308
306
352
CPU
302
336
SINGLE PORT MODULE
337
342
340
338
318
MULTIPORT MODULE
328
334
332
330
326
324
322
320
350

FIG. 3

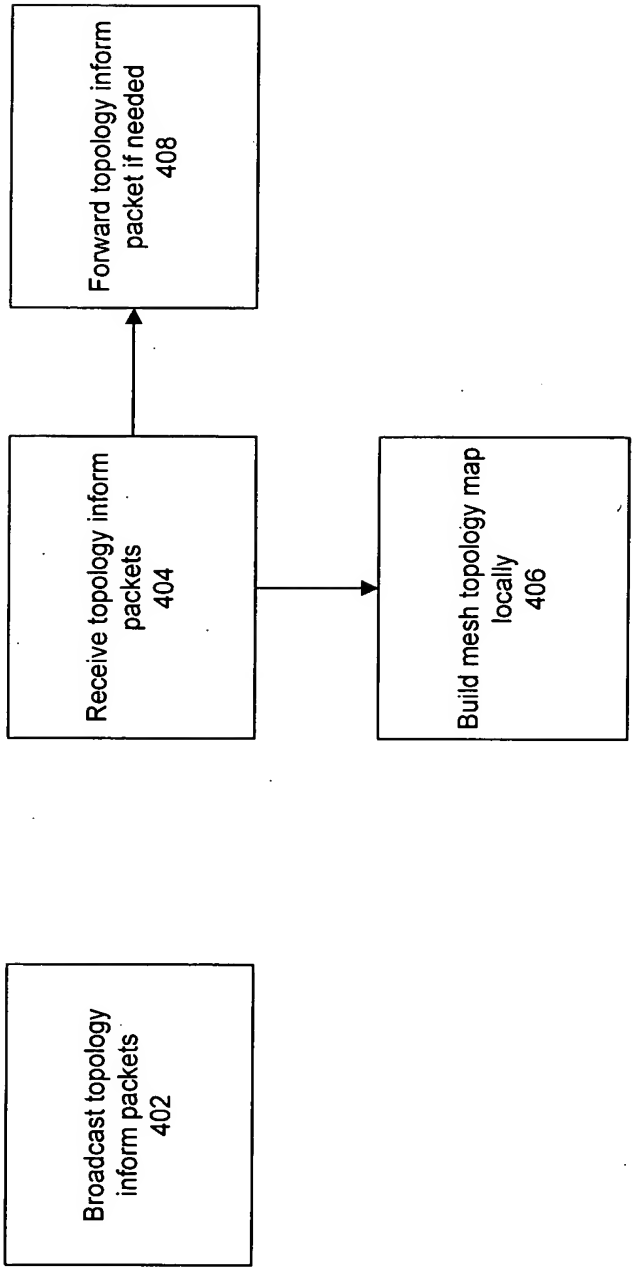

Broadcast topology inform packets 402
Receive topology inform packets 404
Build mesh topology map locally 406
Forward topology inform packet if needed 408

FIG. 4A

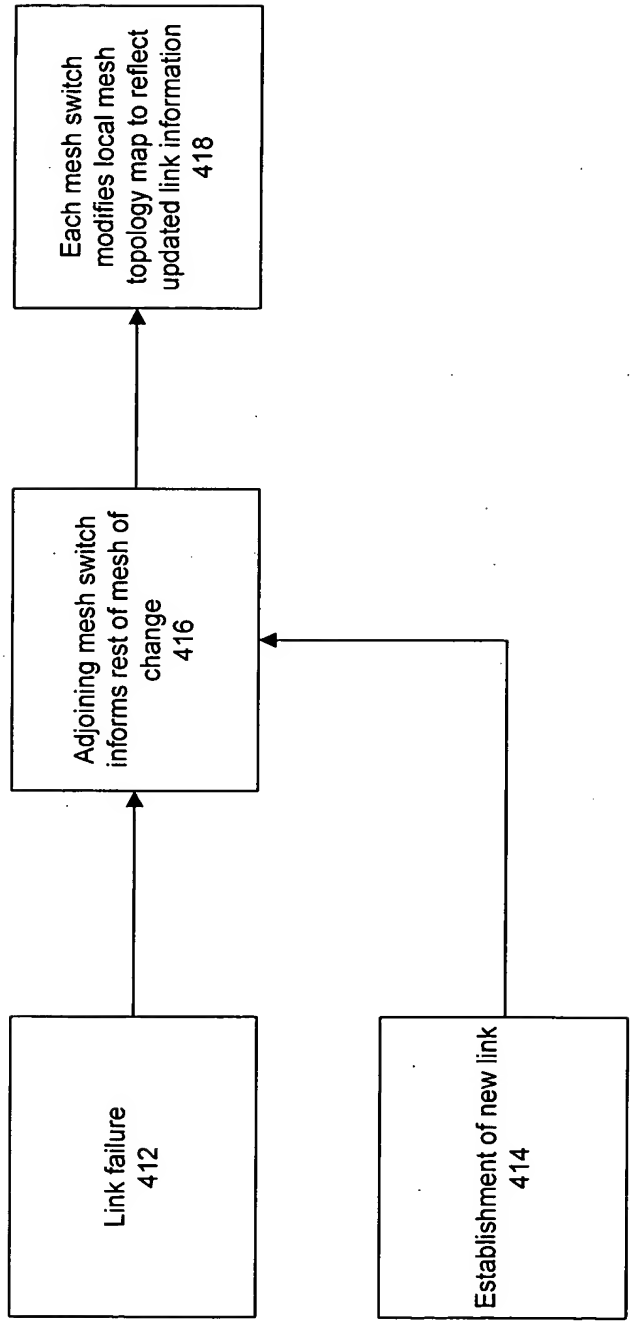

Each mesh switch modifies local mesh topology map to reflect updated link information 418
Adjoining mesh switch informs rest of mesh of change 416
Link failure 412
Establishment of new link 414

FIG. 4B

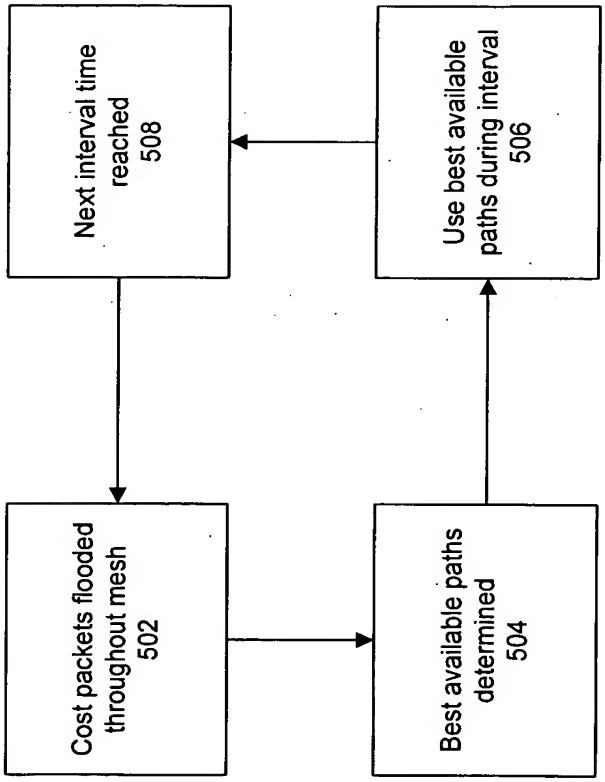
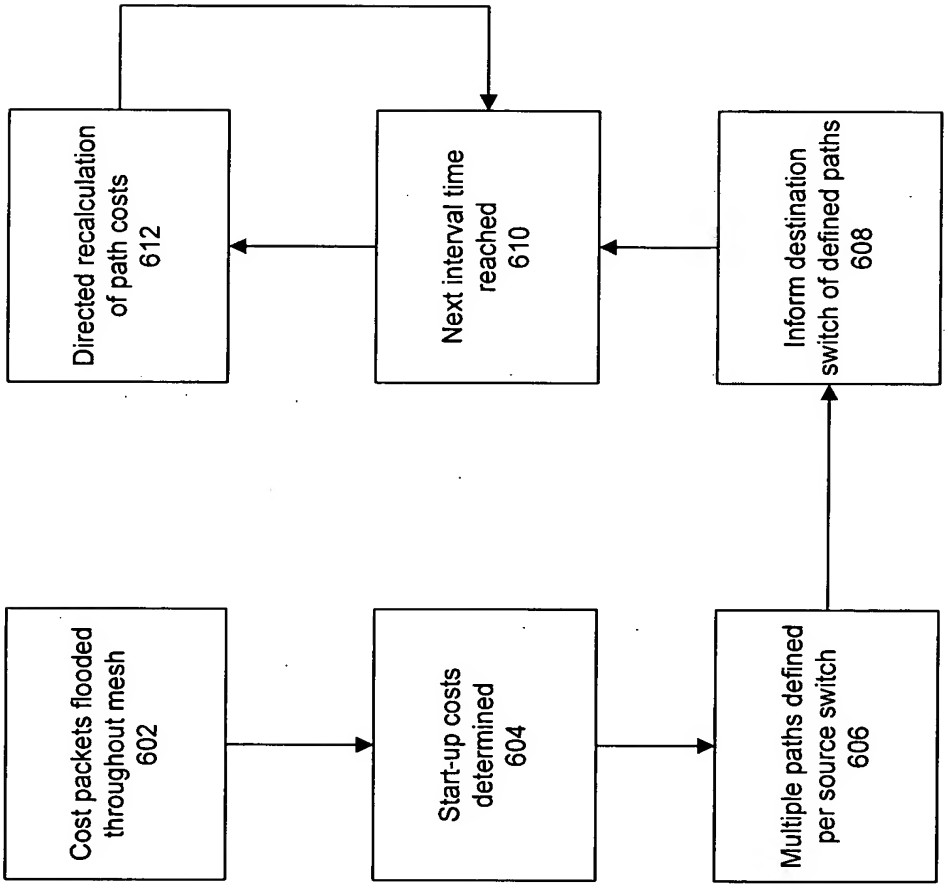

Next interval time reached 508
Use best available paths during interval 506
Cost packets flooded throughout mesh 502
Best available paths determined 504
500

FIG. 5


Cost packets flooded throughout mesh 602
Start-up costs determined 604
Multiple paths defined per source switch 606
Inform destination switch of defined paths 608
Next interval time reached 610
Directed recalculation of path costs 612

600

FIG. 6

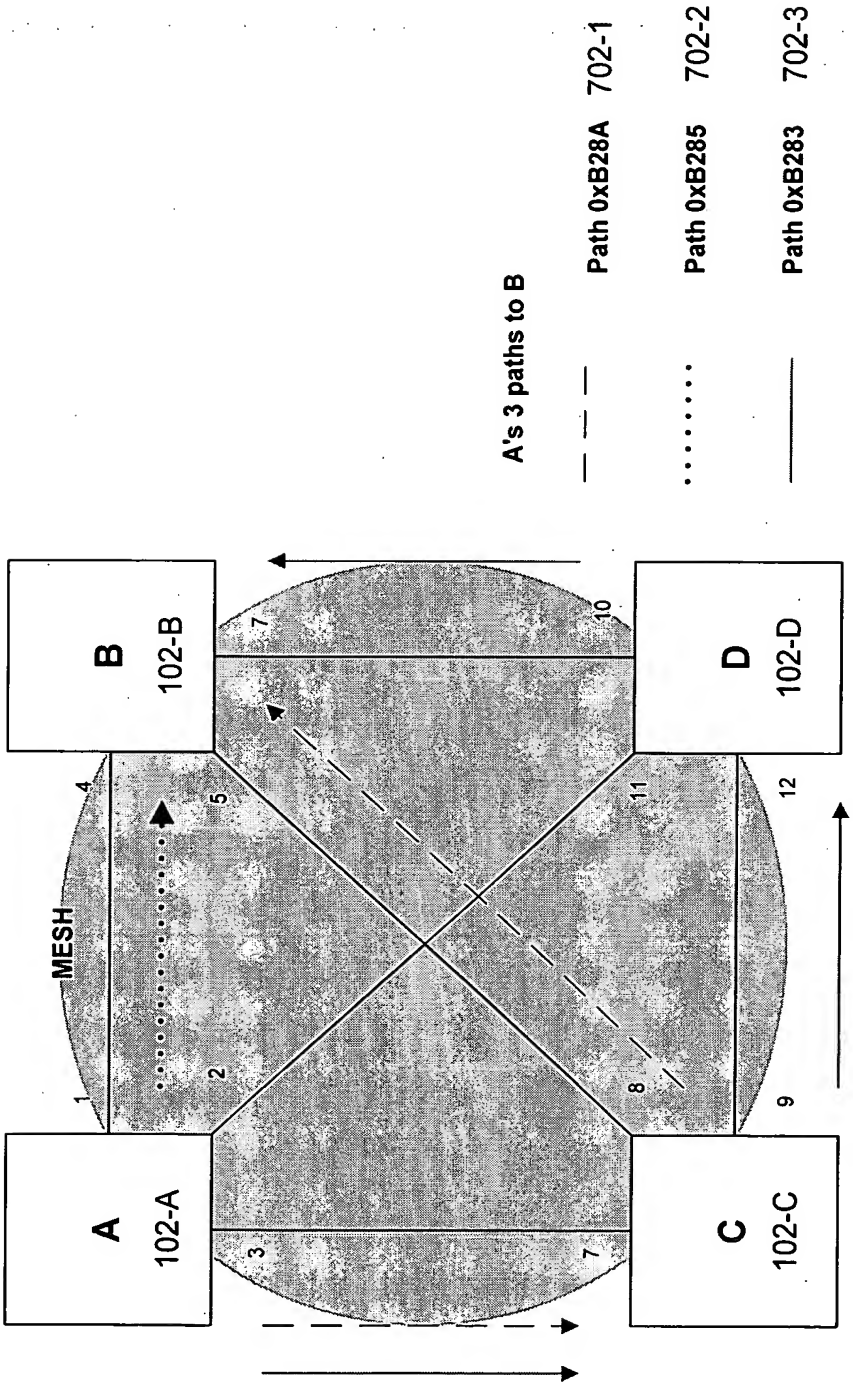

A's 3 paths to B
Path 0xB28A 702-1
Path 0xB285 702-2
Path 0xB283 702-3
A
102-A
B
102-B
C
102-C
D
102-D
MESH
1
2
3
4
5
7
8
9
10
11
12

FIG. 7